REMARKS

Claims 1 through 42 are currently pending in the application.

This amendment is in response to the Office Action of February 19, 2002.

Claims 1 through 42 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gonzalez et al. (U.S. Patent No. 5,323,038) in view of Ohsaki et al. (U.S. Patent No. 5,565,708).

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicants have amended the claims 1, 3, 10, 13, 17, 22, 24, 31, 34 and 38 to clearly distinguish over the cited prior art.

Applicants further submit that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

Turning to the cited prior art, Gonzalez et al. describes an array of finned memory cell capacitors on a semiconductor substrate 52. Stacked capacitor 96 is formed between transistor gates 56, 58 over a first source/drain region 80 functioning as a storage node junction, capacitor 96 being connected to the storage node junction via a layer of first conductive material 82 (see Fig. 10 and col. 3, lines 3-40). Gates 56, 58 include an oxide cap 66 and oxide side wall spacers 74, 78 (see col. 4) A layer of conductive polysilicon 90 and a dielectric layer 92 of silicon nitride cover storage node 86 and portions of cap 66 and side wall spacers 78 (see col. 5, lines 41-58). A contact opening 100 is etched through an interlevel dielectric layer 98 to contact a second source/drain region 80 functioning as an access node junction (see Fig. 12 and col. 5, lines 56-68). A conductive layer of titanium nitride 102 and a tungsten plug 104 fill contact opening 100. Ohsaki et al. teaches a composite trilayer barrier for semiconductor contact holes. The trilayer

barrier is formed by 1) depositing a first titanium layer 5 by sputtering 2) depositing a second columnar grain titanium nitride layer 6 by collimation sputtering and 3) depositing a third titanium layer 13 by sputtering (see col. 11, lines 1-12). The assembly is then heat treated to convert contact portion of titanium layer 5 into titanium silicide layer 7, and to convert titanium layer 13 into thermal titanium nitride layer 13 (see col. 12, lines 44-54).

Applicants respectfully submit the rejections of claims 1 through 42 under 35 U.S.C. § 103(a) because they fail to establish a *prima facie* case of obviousness.

First, there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify Gonzalez et al. with the teachings of Ohsaki et al. as has been presented. Gonzalez et al. involves a stacked capacitor construction that oxidizes side walls 65 of gates 56 and 58 in order to provide more spacing for the contact opening and save a masking step (see col. 1, lines 50-54, col. 2, lines 7-11 and col. 6, lines 1-6). Gonzalez et al. also inserts a layer of conductive material 82 between the storage node junction and the storage node 86 in order to prevent dopant migration into the source/drain region 80 (see col. 1, lines 26-30, col 2, lines 21-24 and col. 6, lines 6-13). Ohsaki et al., on the other hand, is directed to an improved method of forming an electrical connection in a high aspect-ratio contact hole (see col. 9, lines 35-42). Gonzalez et al. overcomes density problems by widening the space for a capacitor contact opening and therefore does not appear to suffer from the aspect ratio issues which Ohsaki et al. seeks to overcome. Furthermore, Gonzalez et al. is concerned with reducing process steps such as masking. Introducing the trilayer barrier of Ohsaki et al. would only add additional process steps into Gonzalez et al which would not be necessary, due to the absence of high aspect ratio contact openings. Accordingly, Applicants respectfully submit Gonzalez et al. teaches away from this combination.

Secondly, Applicants submit the cited references, either alone or in combination, fail to teach or suggest all of the claim limitations. Independent claims 1, 3, 10, 13, 17, 22, 24, 31, 34 and 38, as amended, recite the limitation of a "CVD titanium nitride layer". The sputtered columnar grain titanium nitride layer overlaid with an additional sputtered thermal titanium

nitride layer in the trilayer barrier of Ohsaki et al. do not meet this limitation. Independent claims 1, 10, 22, and 31 recite the limitation of "self-aligned" contact openings. As indicated by Applicants' disclosure, a self aligned contact is one in which the contact plug is immediately adjacent a transistor gate spacer (see specification, page 3, para. 7). Independent claims 3, 13, 17, 24, 34 and 38 recite the limitation of "contact openings at least partially overlapping" the dielectric or silicon nitride layer covering the gate. Gonzalez et al., as modified by Ohsaki et al. does not include self-aligned contact openings or contact openings at least partially overlapping the gate insulator. Rather, the described contact opening 100 is spaced from the gates by interlayer dielectric 98 (see Gonzalez et al. Fig. 12). Independent claims 3 and 24 recite the limitation "said plurality of word lines each having an upper surface and sidewalls covered by a layer of silicon nitride." The cited combination does not teach or suggest this limitation, but rather includes oxide type cap 66 and side-wall spacers 74, 78 (see Gonzalez et al. at col. 4, lines 1-26). A silicon nitride layer 92 is provided as part of the capacitor structure, but it is separated from gates or word lines 56, 58 by cap 66, side-wall spacers 74, 78 and optional layer 90, and further does not extend down the sides of the gate structures (see Fig. 12). Independent claims 13 and 34, and dependent claims 11, 18, 32 and 39, recite a gate insulator dielectric of a first material and an interlevel dielectric of a second material that is selectively etchable from the first material. Gonzalez et al. is silent as to the selectivity between interlevel dielectric layer 98 and cap 66 and side-wall spacers 74, 78.

In view of the foregoing, Applicants respectfully submit the combination of Gonzalez et al. and Ohsaki et al. fails to establish a prima facie case of obviousness under the provisions of 35 U.S.C. § 103(a), and that claims 1 through 42 are clearly allowable over the cited prior art.

Applicants request the allowance of claims 1 through 42 and the case passed for issue.

Respectfully submitted,

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Enclosure: Version with Markings to Show Changes Made

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APPENDIX A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

1. (Twice Amended) A dynamic random access memory array located on a silicon substrate, said array comprising:

a plurality of memory cells, each memory cell including a field-effect access transistor and a stacked capacitor, each field-effect transistor having a first source/drain region functioning as a storage-node junction, each first source/drain region directly connected to the capacitor of each memory cell, each field-effect transistor having a second source/drain region functioning as an access-node junction, having an insulated gate having a lower surface overlying the substrate and insulated therefrom by a gate dielectric layer, having an upper surface, and having vertical sidewalls, said upper surface and said sidewalls being covered by a first dielectric material layer;

an interlevel dielectric layer comprising a second dielectric material, said interlevel dielectric layer blanketing the array to a level above that of the capacitors;

a plurality of digit line contact openings, each contact opening penetrating the interlevel dielectric layer and terminating at an access-node junction, each of said contact openings being self-aligned to the first dielectric material layer, each contact opening being lined with a layer of titanium metal and a layer of CVD titanium nitride located thereover and filled with a CVD tungsten plug; and

a plurality of digit lines formed on top of the interlevel dielectric layer, each digit line making electrical contact to each tungsten plug of a plurality of tungsten plugs.

3. (Twice Amended) A dynamic random access memory cell array located on a silicon substrate, said array comprising:

a plurality of word lines, at least one of said plurality of word lines having a lower surface dielectrically insulated from the substrate by at least one silicon dioxide layer, said plurality of word lines each having an upper surface and sidewalls covered by a layer of silicon nitride;

a capacitor for each memory cell of said dynamic random access memory cell array, each capacitor for storing a charge, the charge stored within each capacitor being accessible by at least one word line of said plurality of word lines;

an interlevel dielectric layer covering the memory cell array and the capacitors thereof;

a plurality of contact openings, each contact opening of the plurality of contact openings penetrating the interlevel dielectric layer to a junction in the substrate, each junction being covered by a titanium silicide layer and located adjacent at least one word line of the plurality of word lines, each contact opening of said plurality of contact openings at least partially overlapping the silicon nitride layer on the sidewall of said at least one adjacent word line, each of said contact openings lined with a CVD titanium nitride layer and at least partially filled with a CVD tungsten plug;

a plurality of digit lines formed on the interlevel dielectric layer, each digit line making electrical contact to each tungsten plug of a plurality of tungsten plugs.

10. (Twice Amended) A dynamic random access memory on a silicon substrate, said memory comprising:

an array of memory cells, each memory cell of said array including a field-effect access transistor and a stacked capacitor, each transistor having a first source/drain region forming a storage-node junction, each first source/drain region being coupled to the capacitor of each memory cell, each transistor having a second source/drain region forming an access-node junction, each transistor having an insulated gate having a lower surface overlying

the substrate and insulated therefrom by a gate dielectric layer, having an upper surface, and having generally vertical sidewalls, said upper surface and said sidewalls being covered by a first dielectric material;

an interlevel dielectric layer comprising a second dielectric material, said interlevel dielectric layer blanketing the array of memory cells to a level above that of the capacitors;

a plurality of digit line contact openings, each contact opening extending through the interlevel dielectric layer and terminating at an access-node junction, each digit line contact opening of said plurality of digit line contact openings self-aligned to the first dielectric material, each contact opening lined with a titanium metal layer, lined with a CVD titanium nitride layer, and filled with a CVD tungsten plug; and

a plurality of digit lines formed on top of the interlevel dielectric layer, each digit line making electrical contact to each tungsten plug of a plurality of tungsten plugs.

13. (Twice Amended) A dynamic random access memory fabricated on a silicon substrate, said memory comprising:

an array of memory cells, each memory cell of said array of memory cells including a stacked capacitor and a field-effect access transistor having a gate electrode overlying the substrate, said gate electrode being dielectrically insulated from the substrate by a gate dielectric layer, said gate electrode having an upper surface and sidewalls covered by a first dielectric material coating;

an interlevel dielectric layer formed from a second dielectric material selectively etchable with respect to said first dielectric material, said interlevel dielectric layer blanketing the memory cell array;

a plurality of contact openings, each contact opening of said plurality of contact openings penetrating the interlevel dielectric layer to a region of the substrate contacting a single access transistor, said region of said substrate covered by a titanium silicide layer, each contact opening of said plurality of contact openings at least partially overlapping said

first dielectric material coating, each contact opening of said plurality of contact openings lined with a CVD titanium nitride layer and at least partially filled with a CVD tungsten plug; and

a plurality of digit lines formed on top of the interlevel dielectric layer, each digit line making electrical contact to each tungsten plug of a plurality of tungsten plugs.

17. (Twice Amended) A dynamic random access memory on a silicon substrate, said memory comprising:

an array of stacked-capacitor memory cells, each memory cell of said array of memory cells having a field-effect access transistor with a channel formed in the substrate and a gate electrode overlying the substrate, said gate electrode having an upper surface and sidewalls covered by a first dielectric material coating;

an interlevel dielectric layer formed from a second dielectric material, said interlevel dielectric layer blanketing the memory cell array;

a plurality of contact openings, each contact opening penetrating the interlevel dielectric layer to a region of the substrate contacting a single access transistor, said region of said substrate covered by a titanium silicide layer, each contact opening of said plurality of contact openings at least partially overlapping the first dielectric material coating on the sidewalls of each gate electrode, each of said contact openings being lined with a CVD titanium nitride layer and at least partially filled with a CVD tungsten plug; and

a plurality of digit lines formed on top of the interlevel dielectric layer, each digit line making electrical contact to each tungsten plug of a plurality of tungsten plugs.

22. (Twice Amended) A memory array on a silicon substrate comprising:

a plurality of memory cells, each memory cell including a field-effect access transistor and a stacked capacitor, each field-effect access transistor having a first source/drain region as a storage-node junction, each first source/drain region directly connected to the stacked capacitor of each memory cell, each field-effect access transistor having a second source/drain region as an access-node junction, each field-effect access transistor having an insulated gate having a lower surface overlying said silicon substrate and insulated therefrom by a gate dielectric layer, having an upper surface, and having vertical sidewalls, said upper surface and said sidewalls covered by a first dielectric material layer;

an interlevel dielectric layer comprising a second dielectric material, said interlevel dielectric layer blanketing said memory array at a level above that of at least one capacitor;

a plurality of digit line contact openings, each contact opening penetrating the interlevel dielectric layer and terminating at an access-node junction, each of said contact openings being self-aligned to the first dielectric material layer, each contact opening being lined with a layer of titanium metal and a layer of CVD titanium nitride thereabove and filled with a CVD tungsten plug; and

a plurality of digit lines formed on top of the interlevel dielectric layer, each digit line making electrical contact to each tungsten plug of a plurality of tungsten plugs.

24. (Twice Amended) A memory cell array on a silicon substrate comprising:

a plurality of word lines, at least one of said plurality of word lines having a lower surface dielectrically insulated from the substrate by at least one silicon dioxide layer, said plurality of word lines each having an upper surface and sidewalls covered by a layer of silicon nitride;

a capacitor for each memory cell of said memory cell array, each capacitor for storing a charge, the charge stored within each capacitor being accessible by the at least one word line of said plurality of word lines;

an interlevel dielectric layer covering the memory cell array and the capacitors thereof;

a plurality of contact openings, each contact opening of the plurality of contact openings penetrating the interlevel dielectric layer to a junction in the substrate, each junction being covered by a titanium silicide layer and located adjacent the at least one word line of the plurality of word lines, each contact opening of said plurality of contact openings at least partially overlapping the silicon nitride layer on the sidewalls of said at least one adjacent word line, each of said contact openings lined with a CVD titanium nitride layer and at least partially filled with a CVD tungsten plug;

a plurality of digit lines formed on the interlevel dielectric layer, each digit line making electrical contact to each tungsten plug of a plurality of tungsten plugs.

31. (Twice Amended) A memory array on a silicon substrate comprising:

an array of memory cells, each memory cell of said array including a field-effect access transistor and a stacked capacitor, each transistor having a first source/drain region as a storage-node junction, each first source/drain region being coupled to the capacitor of a memory cell, each transistor having a second source/drain region as an access-node junction, each transistor having an insulated gate having a lower surface overlying the substrate and insulated therefrom by a gate dielectric layer, having an upper surface, and having generally vertical sidewalls, said upper surface and said sidewalls covered by a first dielectric material;

an interlevel dielectric layer comprising a second dielectric material, said interlevel dielectric layer blanketing the array to a level above that of the capacitors;

a plurality of digit line contact openings, each contact opening extending through the interlevel dielectric layer and terminating at an access-node junction, each digit line contact opening

of said plurality of digit line contact openings self-aligned to the first dielectric material, each contact opening lined with a titanium metal layer, lined with a CVD titanium nitride layer, and filled with a CVD tungsten plug; and

a plurality of digit lines formed on top of the interlevel dielectric layer, each digit line making electrical contact to each tungsten plug of a plurality of tungsten plugs.

34. (Twice Amended) An access memory on a silicon substrate comprising:

an array of memory cells, each memory cell of said array of memory cells including a stacked capacitor and a field-effect access transistor having a gate electrode overlying the substrate, said gate electrode dielectrically insulated from the substrate by a gate dielectric layer, said gate electrode having an upper surface and sidewalls covered by a first dielectric material coating;

an interlevel dielectric layer including a second dielectric material selectively etchable with respect to said first dielectric material, said interlevel dielectric layer blanketing the memory cell array;

a plurality of contact openings, each contact opening of said plurality of contact openings penetrating the interlevel dielectric layer to a region of the substrate contacting a single access transistor, said region of said substrate covered by a titanium silicide layer, and each contact opening of said plurality of contact openings at least partially overlapping said first dielectric material coating, each opening of said plurality of contact openings lined with a CVD titanium nitride layer and at least partially filled with a CVD tungsten plug; and

a plurality of digit lines formed on top of the interlevel dielectric layer, each digit line making electrical contact to each tungsten plug of a plurality of tungsten plugs.

38. (Twice Amended) An access memory on a silicon substrate comprising:

an array of stacked-capacitor memory cells, each memory cell of said array of memory cells having a field-effect access transistor having a channel formed in the substrate and a gate electrode overlying the substrate, said gate electrode having an upper surface and sidewalls covered by a first dielectric material coating;

an interlevel dielectric layer including a second dielectric material, said interlevel dielectric layer blanketing the memory cell array;

a plurality of contact openings, each contact opening penetrating the interlevel dielectric layer to a region of the substrate contacting a single access transistor, said region covered by a titanium silicide layer, each contact opening of said plurality of contact openings at least partially overlapping the first dielectric material coating on the sidewall of a gate electrode, each of said contact openings being lined with a CVD titanium nitride layer and at least partially filled with a CVD tungsten plug; and

a plurality of digit lines formed on top of the interlevel dielectric layer, each digit line making electrical contact to each tungsten plug of a plurality of tungsten plugs.